WHAT IS CLAIMED IS:

1. A core logic chip for use in a personal computer system comprising a system memory and a display, said core logic chip being incorporated therein:

a primary memory control circuit asserting a first read/write signal;

a first data transmission channel in communication with said primary memory control circuit and a first portion of said system memory, transmitting said first read/write signal to said first portion of said system memory;

a graphics accelerator in communication with said display, processing and outputting image data to said display;

a backup memory control circuit in communication with said graphics accelerator, controlled by said graphics accelerator to assert a second read/write signal; and

a second data transmission channel in communication with said backup memory control circuit and a second portion of said system memory, transmitting said second read/write signal to said second portion of said system memory.

2. The core logic chip according to claim 1 wherein said second portion of said system memory includes a frame buffer.
3. The core logic chip according to claim 1 wherein said system memory is a dynamic random access memory.
4. The core logic chip according to claim 1 wherein said first and second data transmission channels are separate from each other and operated independently.
5. A core logic chip for use in a personal computer system comprising a

system memory and a display, said core logic chip being incorporated therein:

a graphics accelerator in communication with said display, processing and outputting image data to said display;

a primary memory control circuit in communication with said graphics accelerator, controlled by said graphics accelerator to assert a first read/write signal;

a first data transmission channel in communication with said primary memory control circuit and said system memory, transmitting said first read/write signal to said system memory;

a backup memory control circuit in communication with said graphics accelerator, controlled by said graphics accelerator to assert a second read/write signal; and

a second data transmission channel in communication with said backup memory control circuit and said system memory, transmitting said second read/write signal to said system memory,

wherein each of said first and said second read/write signals is a part of a specific read/write signal.

6. The core logic chip according to claim 5 wherein said second portion of said system memory includes a frame buffer.
7. The core logic chip according to claim 5 wherein said system memory is a dynamic random access memory.
8. The core logic chip according to claim 5 wherein said first and second data transmission channels are separate from each other but cooperating to transmit said specific read/write signal.